

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A phase locked loop (PLL) circuit using a fractional frequency divider, comprising:

a first PLL stage for controlling the output frequency of a first voltage-controlled oscillator with a deviation, which is obtained by dividing the frequency of the output of said first voltage-controlled oscillator by a first fractional frequency divider and by comparing the frequency-divided output with a first reference frequency [[,]] in a first phase comparator whose output passes through a low-pass filter; and

a second fractional frequency divider for dividing the frequency of the output from the first voltage-controlled oscillator of said first PLL stage;

a second PLL stage for receiving the output of said second fractional frequency divider as a second reference frequency signal.

~~and for inputting the frequency-divided output as a reference frequency signal of a second PLL stage,~~

~~wherein the output signal of a second voltage-controlled oscillator of said second PLL stage is extracted.~~

2. (Currently amended) A phase locked loop circuit using a fractional frequency divider, according to Claim 1,

wherein said second PLL stage is constructed to control the output frequency of said second voltage-controlled oscillator ~~with a deviation, which is obtained by dividing the frequency of the output of said second voltage-controlled oscillator~~ by a frequency divider and by comparing the frequency-divided output from said frequency divider with the second

reference frequency  $[[,]]$  in a second phase comparator whose output passes through a low-pass filter.

3. (Currently amended) A phase locked loop (PLL) circuit using a fractional frequency divider, comprising:

a first PLL stage for controlling the output frequency of a first voltage-controlled oscillator in accordance with a deviation, which is obtained by comparing in a first phase comparator the output of said first voltage-controlled oscillator with a first reference frequency, wherein the output of the first voltage-controlled oscillator passes through a direct digital synthesizer (DDS) for multiplication by  $G/2^h$ ; and

a second PLL stage for controlling the output frequency of ~~said~~ a second voltage-controlled oscillator in accordance with a deviation, which is obtained ~~by using the output of said first PLL stage as a reference frequency signal and~~ by comparing in a second phase comparator the output of  $[[a]]$  said second voltage-controlled oscillator with a signal that is frequency-divided from the output of the second voltage-controlled oscillator by a fractional frequency divider, with the output of said first PLL stage used as a second reference frequency signal,  
wherein frequency division by the fractional frequency divider is expressed by  $1/(m + A/2^b)$ , wherein the value of  $2^{(h-b)}/G$  is equal to a factorial of a positive integer of 10.

~~divided in frequency by a fractional frequency divider, with said reference frequency signal,~~

~~wherein the output signal of a second voltage-controlled oscillator of said second PLL stage is extracted.~~

4. (Currently amended) A phase locked loop (PLL) circuit using a fractional frequency divider, comprising:

a first PLL stage for controlling the output frequency of a first voltage-controlled oscillator with a deviation, which is obtained by frequency-dividing the frequency of the output

of said first voltage-controlled oscillator by a first fractional frequency and by comparing in a first phase comparator the frequency-divided output with a first reference frequency; and

a second PLL stage for controlling the output frequency of ~~said~~ a second voltage-controlled oscillator in accordance with a deviation, which is obtained ~~by using the output of said first PLL stage as a reference frequency signal~~ and by comparing the output of ~~[[a]]~~ said second voltage-controlled oscillator passed through a direct digital synthesizer (DDS) for multiplying the output of said second stage voltage-controlled oscillator by  $G/2^h$ , with said reference frequency signal, with the output of said first PLL stage as a second reference frequency; wherein frequency division by the fractional frequency divider is expressed by  $1/(m + A/2^b)$ , wherein the value of  $2^{(h-b)}/G$  is equal to a factorial of a positive integer of 10.

~~wherein the output signal of a second voltage-controlled oscillator of said second PLL stage is extracted.~~

5. (Currently amended) A phase locked loop circuit using a fractional frequency divider, according to any of Claims 1, 3 and 4 ~~[[to 4]]~~, further comprising:

a band-pass filter inserted into ~~[[the]]~~ a front stage of ~~[[a]]~~ the first phase comparator of said first PLL stage.

6. (New) A phase-locked loop (PLL) circuit using a frequency divider, according to claim 1 wherein said second fractional frequency divider has a frequency division ratio of  $1/(N + C/D)$  to output said reference frequency signal having a frequency of  $(N * D + C)$  Hz.

7. (New) A phase-locked loop (PLL) circuit using a frequency divider according to claim 6 wherein the value of D is a factorial of 2.